

WHAT IS CLAIMED:

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1 1. A method for transferring vector data in a computer system, the method
2 comprising:
3 identifying use of vector data in an application program;
4 implementing at least one vector data instruction for transferring the vector
5 data between a memory and a buffer, the vector data in the buffer being
6 accessible by a processor in the computer system.

1 2. The method of claim 1 further comprising:
2 implementing a synchronization instruction to synchronize accessing the
3 vector data with processing the vector data.

1 3. The method of claim 1 wherein the at least one vector instruction transfers
2 data from the memory to the buffer.

1 4. The method of claim 1 wherein the at least one vector instruction transfers
2 data from the buffer to the memory.

1 5. The method of claim 1 wherein the at least one vector instruction transfers
2 data from the buffer to a general purpose register in the processor.

1 6. The method of claim 1 wherein the at least one vector instruction transfers
2 data from a general purpose register in the processor to the buffer.

1 7. The method of claim 1 wherein the at least one vector instruction is used to
2 determine whether the buffer is available for use.

1 8. The method of claim 1 wherein the at least one vector instruction includes
2 information about a vector stream including the starting address of the vector stream.

1 9. The method of claim 1 wherein the at least one vector instruction includes
2 information about a vector stream including the length of the vector stream.

1 10. The method of claim 1 wherein the at least one vector instruction includes
2 information about a vector stream including the stride of the vector stream.

1 11. The method of claim 1 wherein the at least one vector instruction includes
2 information about a vector stream including the starting address of the buffer.

1 12. The method of claim 1 wherein the at least one vector instruction includes
2 information about a vector stream including the width of the vector data in the data
3 stream.

1 13. The method of claim 1 wherein the at least one vector instruction includes
2 information about whether the vector data is integer or floating point data.

1 ~~SUB A5/~~ 14. A data processing system comprising:
2 a data processor;
3 means for identifying use of vector data in an application program;
4 at least one vector data instruction for transferring the vector data between a
5 memory and a buffer, the vector data in the buffer being accessible by
6 the data processor; and
7 a synchronization instruction to synchronize accessing the vector data with
8 processing the vector data.

1 15. The data processing system of claim 14 wherein the at least one vector
2 instruction transfers data from the memory to the buffer.

1 16. The data processing system of claim 14 wherein the at least one vector
2 instruction transfers data from the buffer to the memory.

1 17. The data processing system of claim 14 wherein the at least one vector
2 instruction transfers data from the buffer to a general purpose register in the processor.

1 18. The data processing system of claim 14 wherein the at least one vector
2 instruction transfers data from a general purpose register in the processor to the buffer.

1 19. The data processing system of claim 14 wherein the at least one vector
2 instruction is used to determine whether the buffer is available for use.

1 20. The data processing system of claim 14 wherein the at least one vector
2 instruction includes information about a vector stream including the starting address
3 of the vector stream in the memory.

1 21. The data processing system of claim 14 wherein the at least one vector
2 instruction includes information about a vector stream including the length of the
3 vector stream.

1 22. The data processing system of claim 14 wherein the at least one vector
2 instruction includes information about a vector stream including the stride of the
3 vector stream.

1 23. The data processing system of claim 14 wherein the at least one vector
2 instruction includes information about a vector stream including the starting address
3 in the vector buffer.

1 24. The data processing system of claim 14 wherein the at least one vector
2 instruction includes information about a vector stream including the width of the
3 vector data in the data stream.

1 25. The data processing system of claim 14 wherein the at least one vector
2 instruction includes information about whether the vector data is integer or floating
3 point data.

1 26. The data processing system of claim 14 further comprising:
2 a vector transfer unit operable to perform burst transfers of the vector data
3 based on the at least one vector instruction.

1 27. The data processing system of claim 14 wherein the means for identifying
2 use of vector data in an application program is a compiler.

1 28. The data processing system of claim 27 wherein the compiler identifies
2 use of the vector data based on whether the vector data is used in a program loop.

1 29. The data processing system of claim 14 wherein the means for identifying
2 use of vector data in an application program includes a vector data indicator, the
3 vector data indicator being recognizable by a compiler as indicating use of the vector
4 data.

1 30. The data processing system of claim 29 wherein the compiler implements
2 the at least one vector transfer instruction when the compiler recognizes the vector
3 data indicator.

1 31. A compiler for handling vector data in an application program,
2 comprising:
3 a source code parser for identifying use of vector data in the application
4 program;
5 an object code generator operable to implement at least one vector data
6 instruction for transferring the vector data between a memory and a
7 buffer when the source code parser identifies the use of vector data, the
8 object code generator being further operable to implement a
9 synchronization instruction to synchronize accessing the vector data
10 with processing the vector data when the application program is
11 executing.

1 32. The compiler of claim 31 wherein the at least one vector instruction
2 transfers data from the memory to the buffer.

1 33. The compiler of claim 31 wherein the at least one vector instruction
2 transfers data from the buffer to the memory.

1 34. The compiler of claim 31 wherein the at least one vector instruction
2 transfers data from the buffer to a general purpose register.

1 35. The compiler of claim 31 wherein the at least one vector instruction
2 transfers data from a general purpose register to the buffer.

1 36. The compiler of claim 31 wherein the at least one vector instruction is
2 used to determine whether the buffer is available for use.

1 37. The compiler of claim 31 wherein the at least one vector instruction
2 includes information about a vector stream including the starting address of the vector
3 stream, and the length of the vector stream.

1 38. The compiler of claim 31 wherein the at least one vector instruction
2 includes information about a vector stream including the stride of the vector stream,
3 and the starting address of the buffer.

1 39. The compiler of claim 31 wherein the at least one vector instruction
2 includes information about a vector stream including the width of the vector data in
3 the data stream.

1 40. The compiler of claim 31 wherein the at least one vector instruction
2 includes information about whether the vector data is integer or floating point data.

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